Multi-Core Class-C Voltage Controlled Oscillator Design

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Abstract

We exploit an idea of coupling multiple oscillators to reduce phase noise (PN) to beyond the limit of what has been practically achievable so far in a bulk CMOS technology. The oscillator is realized in digital 65-nm CMOS as a dual core LC-tank oscillator based on a high-swing class-C topology. As a result of simulation, it is tunable within 1.12-1.25 GHz, while drawing 1.7 mA from a 1.2 V power supply. PN is −135.0 dBc/Hz at 1MHz, respectively, from a 4.07 GHz carrier.

I. Introduction

Voltage controlled oscillators (VCO's) are an essential part of phase-locked loops which are the most common frequency synthesizer. Random fluctuations in the output frequency of VCO's, expressed by phase noise, have a direct impact on timing accuracy where phase alignment is required and cause the signal-to-noise ratio (SNR) issues. In other words, RF oscillators must meet stringent phase noise requirements.

II. Description

To move forward with the PN reduction, we then proceed to the multi-core approach. In general, the presence of N tanks reduces the PN due to a single noise source by a factor N. There are now N current noise sources instead of just one. As the noise sources are all uncorrelated and equal in power, the total PN is N times contribution of one of them. So, the overall PN is N times better than with a single core.

Fig. 1. Chip layout of dual-core high-swing class-C (HSCC) oscillato
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III. Simulation Results

The dual-core HSCC oscillator is implemented in Samsung 65 nm CMOS. Its chip layout is shown in Fig. 1. The measured output frequency range is from 1.12 GHz to 1.25 GHz, yielding 10.8% tuning range. Simulated phase noise (PN) is plotted in Fig. 2. In case of a dual core, the R_P value is half, so the PN is reduced by 3dB compared to a single core.

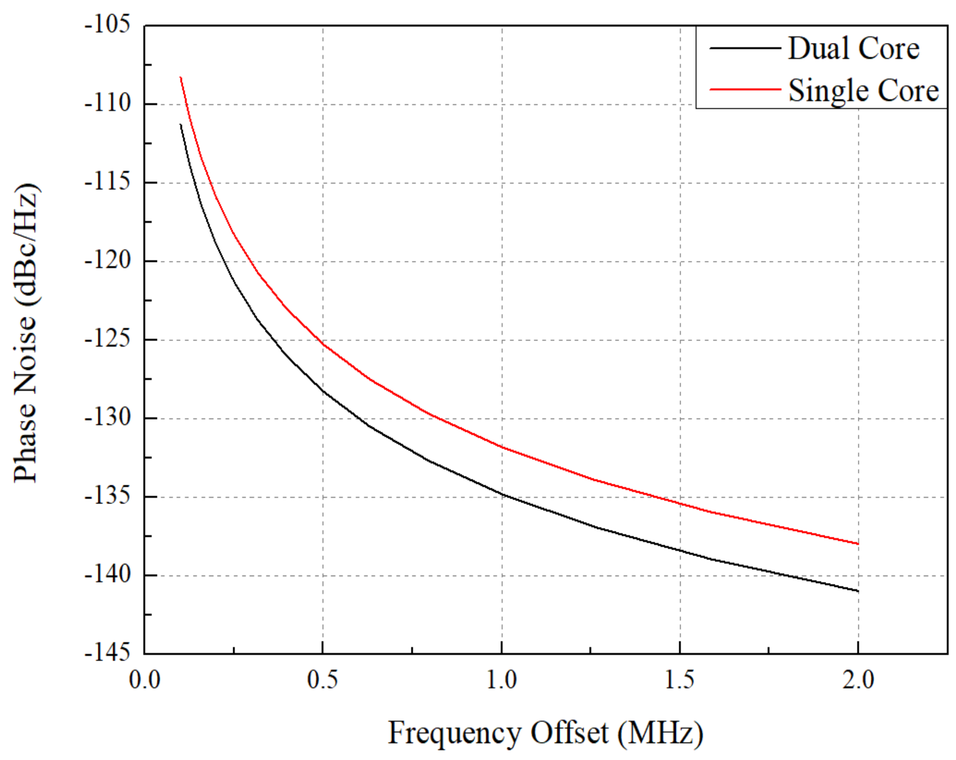

Fig. 2. Simulation plot of phase noise of dual-core oscillator and single-core oscillator.

Acknowledgement

This work was supported by Institute for Information & communications Technology Promotion grant funded by the Korea governmet,
and in part by the IDEC.

ISOCC 2020 Chip Design Contest
This work was supported by the IDEC